A THEORETICAL IMPLEMENTATION WITH PHYSICAL DESIGN OF V-DIODE

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ABSTRACT

Main focus of the paper is based upon the conduction phenomena and the energy band formation characteristics of the novel device, which is named as v-diode i.e. variable diode. The concept of this diode is based upon the basic semiconductor physics. This device can operate in both biasing: forward and reverse. Here semiconductor characteristics inversion is used to achieve the v-diode characteristics. This diode operates as n-p diode and in some cases acts as p+ i n+ diode depending on the biasing polarity. Mainly the energy band formation, band energy changing characteristics are discussed here broadly. All the calculations justifies the device characteristics and band-gap modulation technique of this diode. The fundamental expressions of diode have used here and some auxiliary equations have derived from those expressions to achieve the working characteristics of this device. This paper is presented theoretically along with the all clarifications about the major characteristics of the v-diode like energy, potential and current. The COMSOL MULTIPHYSICS and MATLAB have used to generate the graphical plots for technical justification of v-diode.

KEYWORDS

1. INTRODUCTION

Diodes have been most popular and essential device in the present electronic world since 1874, with its discovery. Along with every day's thinking and the refinement of science and need for the new up-gradation challenge, various types of developing have done on the diodes continuously, likely to tunnel diode, zener diode, schottky diode etc. Here a very new kind of discovery on the diode is proposed theoretically in this paper, which is named as v-diode. As the diode shows the energy characteristics graph as the English 22th alphabet v, this is the main reason of nomenclature of this device as v-diode. The design of the diode has done in such a way that it would be eligible to operate itself in both bias such as forward and reverse.

In this device a special phenomenon of semiconductors is used, which is semiconductor inversion phenomena. Due to a specified biasing at a specified time the doped semiconductors automatically gets inverted. This inversion of the diode characteristic at different biasing makes this device more versatile. Often the device behaves as n-p diode and sometimes behaves as p+ -i-n+ diode [1]. These overview would be more precise from the characteristics graphs and from all the calculations those have been attached in the paper for the justification of the device characteristics. Mostly focused on the energy developing criteria individually for the each semiconductor segments and also the current flowing criteria of this diode is briefly explained with proper equations and simulations. The calculations regarding energy and currents have done intently for the justification of this theoretical device. All the expressions are validated by graphical plotting using MATLAB, in section VI [2]–[4]. Other energy band schematic diagrams have sketched by paint. The device time delays are also discussed inside. The successive demonstration and the result of this paper will contribute a high and new technical information to the modern electronic industry.

In the following section II, the semiconductor band energy formation technique is approached. Where the basic energy band theory of semiconductors is mentioned. Section III presents the diode behavior in different biasing applications along with diagrams and mathematical equations. In section IV the v-diode graph generation due to energy band effect is shown and section V gives all the mathematical calculations regarding the biasing effects. Section VI contains the graphical verification of the illustrated equations in previous section.

2. THEORETICAL EXPLANATION OF THE DEVICE ENERGY BAND FORMATION

This device is formed upon four segments of doped semiconductors. Let's have a discussion about the first segment p+ semiconductor region, which is highly doped with acceptor ions. This highly doping signifies the level of existing holes inside the semiconductor material. Hence according to the Fermi's energy level, the energy level for the p+ substrate $F_{E_{p+}}$ would be just above of the valance band but below intrinsic energy level F_{E_i}, as fig. 1. So the energy difference between the valance band (V.B) and the actual energy $F_{E_{p+}}$ of the doped semiconductor is naturally very low. That means they are very closer together, as shown in fig. 1 [5].

Secondly about the n+ semiconductor which is the last segment of this device. It is nothing but the highly doped n-type semiconductor region, which is denoted as n+ region. Here the Fermi's energy level $F_{E_{n+}}$, is very closer with the conduction band, as fig. 1. So, for that the energy difference is very less between the conduction band and Fermi's energy level of n+ [6].
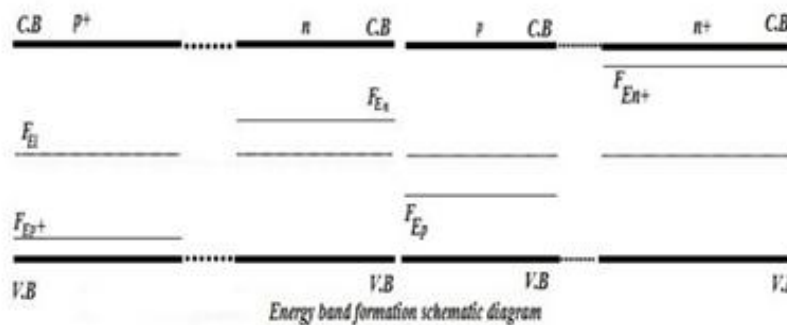

Energy band formation schematic diagram

Figure 1

Fig. 1.Energy bands at zero biasing

The n-type and p-type semiconductors those are placed just between the p+ and n+ region. This n-p region can be called as joiner of other two regions/segments. This special type of construction have made this device versatile [7].

The actual band energy model of the v-diode is shown in fig. 1. At the very left side the p+ segment and at very right side n+ segment is situated. The other two segments are n-p, those are implemented between two heavily doped semiconductors. Hence the n-p junction is literally having low energy level compared to other two semiconductor materials [8]. This n-p junction is to be implemented because of the interconnection between other two regions. In the sense of biasing later this n-p junction will control fully the semiconductor band energy inversion phenomena. This region should be very thinner compared to other semiconductor segments. Mainly it is the one of the live reason to have lesser energy of the n-p region. If this energy criteria is graphically plotted, as fig. 5, then it is seen that at the most left side in p+ region is

having a higher energy level due to hole concentration and at the n+ region there is also having higher energy due to electron concentration (according to the Solid State Device Physics) [9]. And the intermediate regions, n and p, the energy level is lesser than other two regions, as explained before. Here the linearity of graph is considered for the creation of the 'v' energy graph. From the zero displacement point as can be displaced towards the junctions of doped semiconductors form one side to another, the energy level would be decreased gradually. So there would be a possibility to have a graph like v, fig. 5. This phenomena indicates that how the energy of the entire device varies from one terminal to another terminal of the device [10].

3. REPRESENTATION OF DIODE BEHAVIOUR IN DIFFERENT BIASING

A. Reverse bias operation

Elaboration for p+ n junction: In reverse bias firstly when the p+ and n+ regions would be biased by negative and positive potential respectively (here n type semiconductor is assumed as virtually connected with positive potential), then at the very beginning time of biasing, the diode would be acted as a reverse diode. Means ideally no conduction phenomena would be noticed [11]–[13]. Along with some time delay after biasing, the energy level of the p+ semiconductor would be started to decrease. After a certain moment (t), as explained in section V, the energy band of the p+ semiconductor $F_{E_{p+}}$, would be very closer to the energy band level of n-type semiconductor is F_{E_n}, as explained in section V. When the two energy band level of two semiconductors p+ and n, would be ideally overlapped then the total segment of semiconductor, p+ and n, would be changed into the single type semiconductor i.e. n-type due to upward energy band shifting, as fig. 2. Here it is said to be that the p+ doped semiconductor has got inverted to the n-type semiconductor.
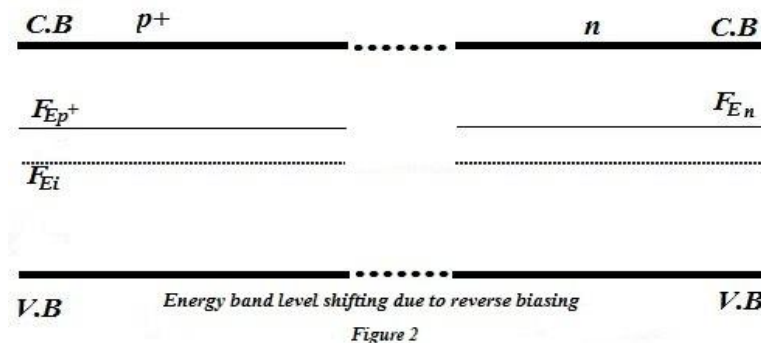

Fig. 2.Energy band shifting of p+ semiconductor towards n semiconductor

From the fig. 2, it is clear to say that the energy band level of p+ semiconductor has been shifted upward by some external energy i.e. E_3 (E_3 is explained briefly is section V) and it is nearly equal to the band level of the n-type semiconductor [14]. Here E_3 energy is conducted as a driving energy by which the $F_{E_{p+}}$ band has drove up to F_{E_n} energy band.

Elaboration for p n+ junction: The next phenomena is the inversion of the n+ semiconductor into the p-type semiconductor, which is approximately same with the p+ to n semiconductor inversion phenomena, as discussed in previous section. It is well known that in case of n+ semiconductor, the Fermi's energy level stays just below of the conduction band (C.B), fig. 1. But when the n+ semiconductor is introduced with a positive potential, then the energy band level of the n+ semiconductor would be tried to get closer with its valance band (V.B) gradually [15]. The positive bias is said to be the flowing of holes, so the holes (h+) would be started to

accumulate inside the n+ region. Severally the band energy level would be started to migrate towards the valance band from the conduction band. As a conclusion of this migration is said to be that the total n+ semiconductor would be changed into the p-type semiconductor gradually, when the Fermi's energy band level of n+ semiconductor $F_{E_{n+}}$ would be ideally overlapped with the energy level of p type semiconductor F_{E_p}, as fig. 3 [16]. In previous section the one segment is noticed as n-type and here another segment changed into p-type caused by reverse bias. Hence the whole diode can be considered as n-p semiconductor diode, which was p+ n-p n+ semiconductor diode previously. These theoretical explanations are successively verified with a rigid mathematical calculation in section V (subsection B) [17].
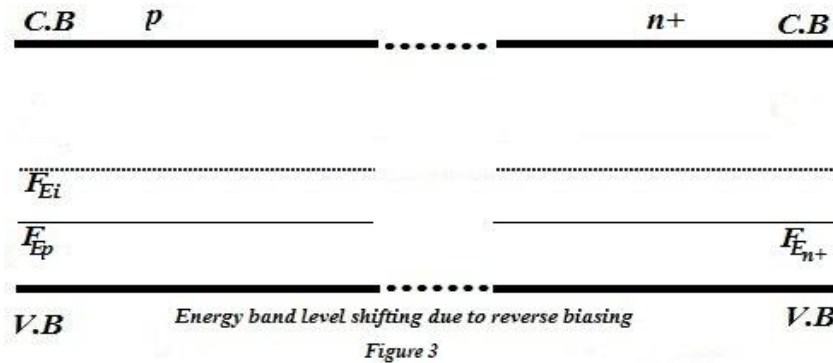

Fig. 3.Energy band shifting of n+ semiconductor towards p semiconductor

B. Forward Bias operation

In the sense of the forward biasing, the device terminals should to be connected with a forward e.m.f. So for that the p+ semiconductor region is to be affected by a positive (+ve) potential and the n+ semiconductor segment to be introduced with the negative (-ve) potential. Form the atomic view of the device it can be said that the electrons (e^-) would be pushed heavily into the n+ region as well as the holes (h+) would be pushed into the p+ region towards the junctions. After that all the immobile ions at every junctions would be started to recombine with the opposite charges rapidly [18], [19]. As the potential increases this effect also increases. Hence the n-p segment width would be reduced and this segment would become an intrinsic semiconductor region [20]. This causes the changing of the device into p+ n+ junction diode gradually, as fig. 4. Now the n-p segment that should be considered as an intrinsic region, which is nothing but an internal energy level controller between p+ and n+ semiconductors. In the intrinsic part the number of holes would be approximately equal to the number of electrons. This intrinsic region is to be denoted as I layer [10] as fig. 4. Because all the minority charge carriers have been recombined with the majority charge carriers through the region. Hence the intermediate portion of the p+ and n+ semiconductor is to be conducted as an intrinsic semiconductor junction only [21]. So the whole device would be converted into 'p+ -i- n+' junction diode within a certain interval of time after biasing, as fig. 4.
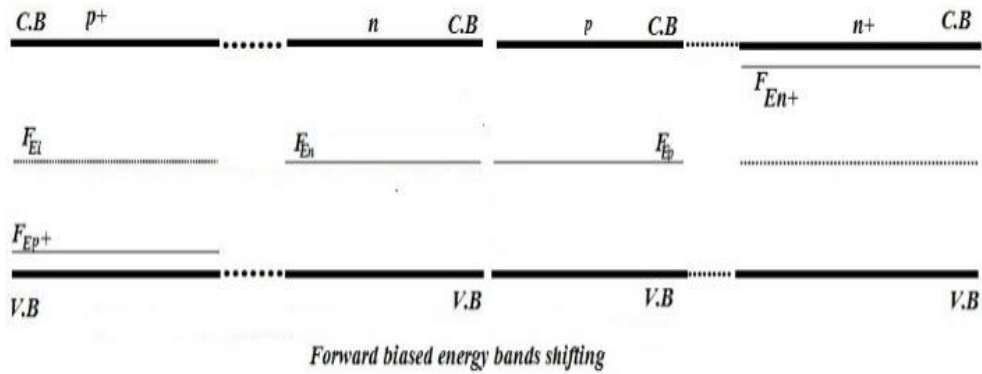
Forward biased energy bands shifting

Figure 4

Fig. 4.Energy bands in forward bias and I layer formation

This p+ -i- n+ characteristics current is denoted as,

$$I_f = Aq \in (\mu_p p + \mu_n n)$$

Hence the μ_p and μ_n are the motilities of the carriers holes and electrons respectively. Previously explained the area of the n-p segment is very less. From above equation, compared to the area of the respective n-p segment, the forward current I_f would be less [22], [23].

On the application of forward bias, carrier injection into the I layer from the p+ and n+ reduces its forward resistance. However, in the I region the carrier concentrations diminishes the width depth due to recombination. This causes the carrier concentrations to rise much above their equilibrium values thereby result in reduced forward resistance again.

$$R_f = \frac{W}{\sigma A};$$

Along with the decreasing phenomena of the junction width (W) the forward resistance also decreases [24].

But the concentration of the holes and the electrons remain almost equal through the I layer. This phenomena recovers the reducing of forward current.

4. REPRESENTATION OF ENERGY VARIATION CRITERIA AND GRAPHICAL JUSTIFICATION USING COMSOL MULTIPHYSICS

According to the energy bands theory as recommended in standard Solid State Device Physics, the generation of energy band of this device has been plotted in fig. 5 [25]. Considering the total energy condensation criteria of the device, this plotting has done intently, which signifies the energy band characteristics of v-diode. While the linear displacement 'x' is increases along with the X-axis toward the junctions, it is seen that sometimes the energy characteristics have depleted. Because of having different energies at the every junctions (considering as homo junction), as explained in section II. For that the energy curve is varied [26]. Starting from the p+ semiconductor and ending at the n+ semiconductor it is seen that the linear energy curve have got changed for two times. First one is decreasing phenomena, as segment 'v1'. Which signifies the energy variation between the p+ and n junction. Secondly another segment of the curve is denoted

as 'v2', which signifies the energy variation though the junction between p and n+ region. Here the energy increasing phenomena is shown. The plot of the energy incremental and decrementing phenomena have shown in fig. 5. After cascading those two segments of energy variation graph, it can be conclude that the graph characteristics is likely to the English 22th alphabet v, as fig. 5 [27]–[29].
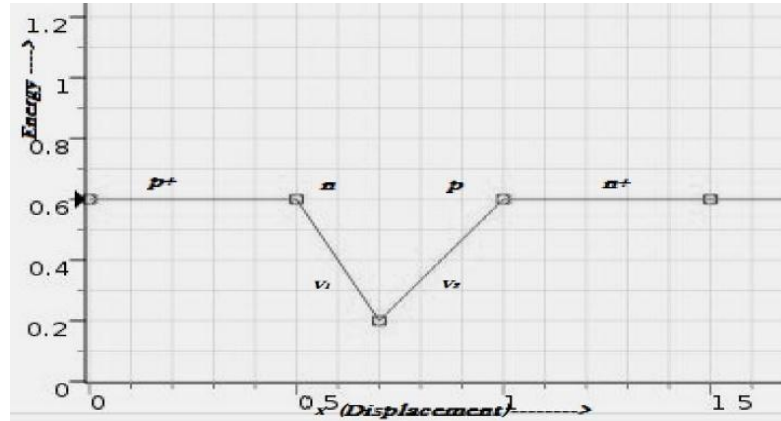

Fig. 5.V energy graph

5. PROSPECTIVE CALCULATION ON ENERGY, POTENTIAL AND TIME DELAY

A. Explanation of semiconductor band energy and working time delay

Considering the energy of p+ region is E_2 and the energy of n region is E_1, the net energy difference is indicated as E_3, which can be written as $E_3 = E_2 - E_1$. Here the maximum calculation is purely referred by the density state concept. For the hole density i.e. the density of the acceptor atom is indicated as N_a, and the density of state of the electrons i.e. donor atoms have taken as N_d [30]. This method of density states is continued through the calculations. On the behalf of the energy E_1 the corresponding potential is taken as $\emptyset_1$ and as well as $\emptyset_2$, $\emptyset_3$ for the respective energies E_2 and E_3.

Hence, $E_3 = E_2 - E_1$

$$\emptyset_3 = \emptyset_2 - \emptyset_1$$

$$= \frac{kT}{e} \ln \frac{N_a}{n_i} - \frac{kT}{e} \ln \frac{N_d}{n_i}$$

$$= \frac{kT}{e} \ln \frac{N_a}{N_d}$$

$$e\emptyset_3 = kT \ln \frac{N_a}{N_d}$$

$$E_3 = E_0 \ln \frac{N_a}{N_d}$$

$$E_3 = E_T \ln \frac{N_a}{N_d} \; [E_0 = E_0] \tag{1}$$

$$E_T = \frac{E_g}{\ln\frac{N_a}{N_d}} \tag{2}$$

Here, $e = 1.602 \times 10^{-19} C$ which is nothing but single electronic charge. Assuming the life time of the carriers at p+ and n junction is τ, the relation between the energy of p+ semiconductor E_2 and with the initial energy is supposed to E_0 is expressed by eq. 3 [31]. This E_0 is defined as the energy which develops normally due to the thermal effect. This thermal energy is also can be said as E_T. The relation between these two energies is shown below,

$$E_2 = E_0 e^{-\frac{t}{\tau}} \tag{3}$$

As a solution of this equation, the expression of the time t justifies that, the required time to reach the Fermi's energy level of the p+ semiconductor to the Fermi's energy level of the n type semiconductor. This expression is modified as,

$$t = \tau \ln\frac{E_T}{E_2} \tag{4}$$

Hence the thermal energy and the initial energy is taken as same with each other's i.e. $E_T = E_0$. After replacing the E_T value the re-moderated equation is expressed as [32]–[34],

$$t = \tau \ln\frac{E_g}{E_2 \ln\frac{N_a}{N_d}} \tag{5}$$

After replacing all the energies by potentials from eq. 5, the actual expression is given as,

$$t = \tau \ln\frac{\emptyset_g}{\emptyset_2 \ln\frac{N_a}{N_d}} [E = e\emptyset] \tag{6}$$

This relation acts for the time required for the Fermi's energy level of p+ region to reach up to the Fermi's level of n region energy level, which is denoted by t. As the biasing would be more increased the donor atoms i.e. the minority atoms (e^-) would be decreased. Hence value of N_d would be diminished. In account of that type of phenomena the time would be decreased with decreasing of N_d.

B. Explanation of current flowing criteria using prospective calculations

Before explaining the current flowing criteria of v-diode, the main thing is to be focused, that this diode firstly will not be behaved like any normal diode in bias. But after some moments it would be seen that the diode would follow the natural diode characteristic phenomena which is nothing but the Shockley diode equation characteristic. The whole theory has briefly explained by proper equations afterwards.

First of all when the diode would be biased there would have a certain reverse phenomenon, as explained in section III. In that case there must to have reverse saturation current which is denoted by I_r. At every junctions there must have some capacitance effect. Which would have certain time constant τ, from section V (subsection A). As explained previously this time constant is the life time of carriers at junctions. If the actual forward diode current is indicated by I_f, then the net current through the whole diode with the respective time t is represented as [35],

$$I(t)=I_f-I_re^{-\frac{t}{\tau}} \tag{7}$$

Having time dependency of the diode current, for calculation purpose exponential term is multiplied with the reverse saturation current I_r. This is taken because, elongation with time the reverse current decreases.

$$I(t) = I_r\left(e^{\frac{E}{\eta kT}} - 1\right) - I_re^{-\frac{t}{\tau}}$$

$$=I_r\left(e^{\frac{E}{\eta kT}} - 1 - e^{-\frac{t}{\tau}}\right) \tag{8}$$

Case 1: At the very first of biasing, i.e. absolutely the beginning of biasing, the time can be treated as a condition t=0.

So, $$I(0)= I_r\left(e^{\frac{E}{\eta kT}} - 2\right) \tag{9}$$

Hence, if driving energy is not provided, means at initial condition the input is zero. So E=0, because of the input potential is, V=0.

$$I(0) = -I_r$$

Negative sign signifies the direction of current. Hence the current is reversely directed.

Case 2: Next condition is the t= τ,

$$I(\tau)= I_r\left(e^{\frac{E}{\eta kT}} - 1 - e^{-1}\right)$$

$$=\frac{I_r}{e}\left(e^{\frac{E+\eta kT}{\eta kT}} - e\right) \tag{10}$$

Case 3: As a last condition t=∞. Hence the time is infinite stands for that, the observation after a long time of the biasing. This expression is re-modified as, from eq. 8,

$$I(\infty)=I_r\left(e^{\frac{E}{\eta kT}} - 1\right) \tag{11}$$

This eq. 11 is nothing but the Shockley diode characteristic equation. Hence this can be concluded as after a long time of conduction the v-diode would be converted into a normal p-n junction diode, as explained theoretically in section III. This is the mathematical expression for the justification of the previous explanation [36].

6. MATLAB GRAPHICAL VALIDATIONS OF THE EXPRESSIONS

A. Graphical validation of expression 8

Fig. 6 shows the diode current flowing phenomena with potential variation. The output current is denoted by $I(t)$, which is time variant in nature. Hence to obtain this plot some arbitrary values have taken as follows:

Operating temperature 30°C; reverse saturation current I_r=0.2 μA; η=1 for Ge. The used potential range is 0-20V and the range of operating time have taken as same with potential range [37].

The standard life time of the carriers (10^{-8} sec) have used as the value of τ. If the life time is beyond of this provided time value, then the junctions would be flooded.

It is seen from the graph that after a long time the output is plotted. Until the potential 18V is achieved the device could not be able to show any current characteristic. For that the output current is still absent beyond the 18V potential. But after that a certain current phenomena is noticed, as fig. 6. When potential is given at the initial moment to the device, it undergoes into a non-conducting zone. After a certain moment the device started to conduct. This following figure justifies that this device will not show the diode characteristic properly at the first time of biasing. This step is for the semiconductor inversion phenomena [38].
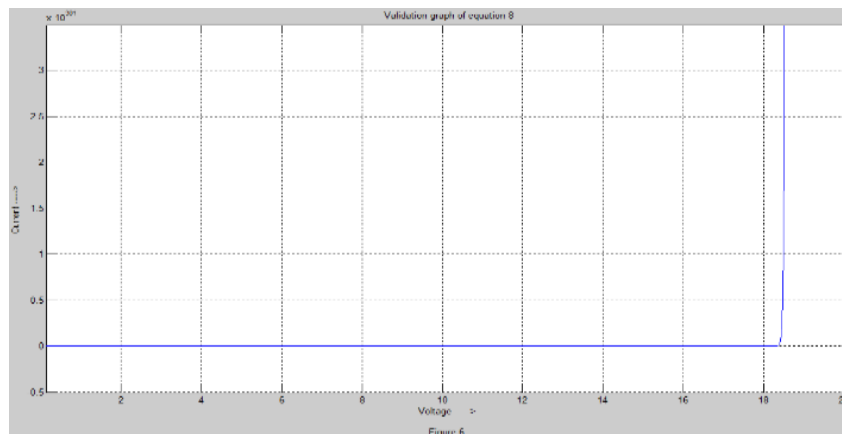

Fig. 6.Validation of device current within a certain

B. Graphical validation of expression 11

As the matters have discussed in previous sub-section B, about the long duration conduction phenomena, the diode would show a characteristics graph like a normal p-n junction diode. Also mentioned theoretically the graphical characteristic would follow the Shockley diode equation. Hence to justify this theory, the corresponding equation 11 needs to be verified properly [39]. In the fig. 7, the characteristic of the equation is successfully verified. To generate this graph those values have selected, are same with the values had used to generate figure 6. Only two differences are to be head lighted i.e. the potential range has considered as 0 to 0.5V with a step size/interval 0.001. And the time is assumed as a long duration. Hence it is to be said that this graph shows the diode characteristic as Shockley diode equation [40].

According to this graph it is successfully concluded that the device behaves as n-p diode after certain time delay from the biasing.
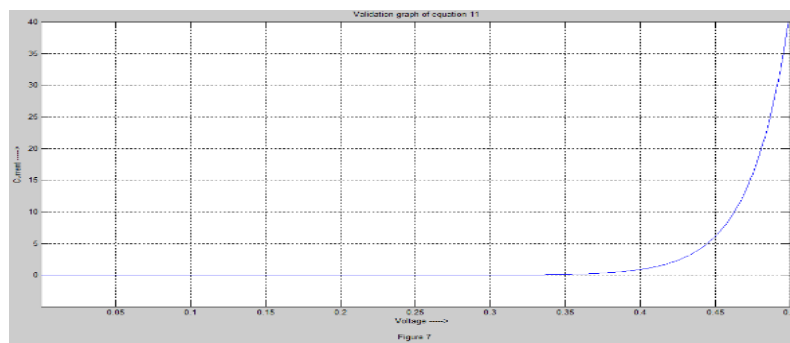

Fig. 7. Graphical justification of device inversion phenomena

7. CONCLUSIONS

The propound design of the v diode is a new type of approach to the world of diode. In the above theoretical presentation of the characteristics of v diode it is repeatedly seen that this diode can operate in both biasing. But there is having different output approach of the device. Under different biasing there semiconductor inversion phenomena is introduced, which is liable for inversion of the device semiconductor zones. In section V the time delay of the device has been calculated corresponding with the semiconductor region potentials and density of states. Which provides the time required for the diode to change itself into another form after a fixed type of biasing. In the subsection B the derived equations are justifying the current flowing measurement of the device with respect to the time. Three cases are considered for the calculation and at last it is seen that after a long time period of biasing the device would follow the Shockley diode equation. That current is denoted by eq. 11. Next in section VI the equations have justified by plots. For the generation of the plots arbitrary values have taken. As operating temperature $30°C$ the fig. 6 shows the graph which is keen dismissed from Shockley diode characteristic. But in fig. 7 it is seen that the diode characteristic is perfectly identical with the Shockley diode graph. Since it needs to be concluded as at the time inversion of semiconductors from one form to another one the diode will not show the Shockley diode characteristic, but after a time delay it will behave as a normal diode dependent on the specified biasing. If forward bias is applied then it will play as a p+ -i- n+ diode. And if reverse bias is applied then it will play as n-p semiconductor diode. As a future direction this device could be used rapidly when some versatile applications are needed.

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